

DS90LV028A

DS90LV028A 3V LVDS Dual CMOS Differential Line Receiver



Literature Number: SNLS013D

DS90LV028A

3V LVDS Dual CMOS Differential Line Receiver

General Description

The DS90LV028A is a dual CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

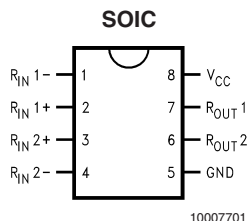
The DS90LV028A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver also supports open, shorted and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV028A has a flow-through design for easy PCB layout.

The DS90LV028A and companion LVDS line driver provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

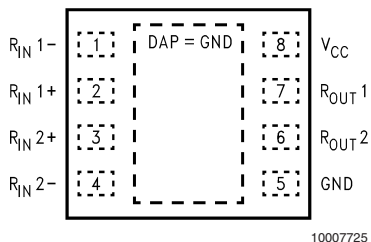
- >400 Mbps (200 MHz) switching rates
- 50 ps differential skew (typical)
- 0.1 ns channel-to-channel skew (typical)
- 2.5 ns maximum propagation delay
- 3.3V power supply design
- Flow-through pinout
- Power down high impedance on LVDS inputs
- Low Power design (18mW @ 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) differential signal levels
- Supports open, short and terminated input fail-safe
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial temperature operating range (-40°C to +85°C)
- Available in SOIC and space saving LLP package

Connection Diagrams



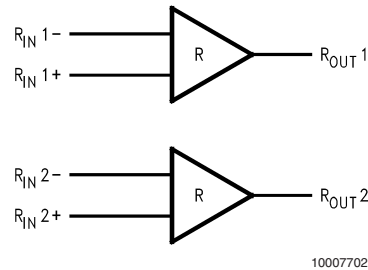
Order Number DS90LV028ATM
See NS Package Number M08A

LLP (Top View)



Order Number DS90LV028ATLD
See NS Package Number LDC08A

Functional Diagram



Truth Table

INPUTS	OUTPUT
$[R_{IN+}] - [R_{IN-}]$	R_{OUT}
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L
Full Fail-safe OPEN/SHORT or Terminated	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.3V to +4V
Input Voltage (R_{IN+} , R_{IN-})	-0.3V to +3.9V
Output Voltage (R_{OUT})	-0.3V to $V_{CC} + 0.3V$
Maximum Package Power Dissipation @ +25°C	
M Package	1025 mW
Derate M Package	8.2 mW/°C above +25°C
LD Package	3.3W
Derate LD Package	25.6 mW/°C above +25°C
Storage Temperature Range	-65°C to +150°C

Lead Temperature Range Soldering

(4 sec.)

+260°C

Maximum Junction Temperature

+150°C

ESD Rating (Note 4)

(HBM 1.5 kΩ, 100 pF)

≥ 7 kV

(EIAJ 0Ω, 200 pF)

≥ 500 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		3.0	V
Operating Free Air Temperature (T_A)	-40	25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units	
V_{TH}	Differential Input High Threshold	$V_{CM} = +1.2V, 0V, 3V$ (Note 12)	R_{IN+}			+100	mV	
V_{TL}	Differential Input Low Threshold		R_{IN-}	-100			mV	
I_{IN}	Input Current	$V_{IN} = +2.8V$ $V_{CC} = 3.6V$ or $0V$		-10	±1	+10	µA	
				-10	±1	+10	µA	
		$V_{IN} = +3.6V$ $V_{CC} = 0V$		-20		+20	µA	
V_{OH}	Output High Voltage	$I_{OH} = -0.4$ mA, $V_{ID} = +200$ mV	R_{OUT}	2.7	3.1		V	
		$I_{OH} = -0.4$ mA, Inputs terminated		2.7	3.1		V	
		$I_{OH} = -0.4$ mA, Inputs shorted		2.7	3.1		V	
V_{OL}	Output Low Voltage	$I_{OL} = 2$ mA, $V_{ID} = -200$ mV			0.3	0.5	V	
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$ (Note 5)			-15	-50	-100	mA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA			-1.5	-0.8		V
I_{CC}	No Load Supply Current	Inputs Open	V_{CC}		5.4	9	mA	

Switching Characteristics

$V_{CC} = +3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$ (Notes 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
t_{PHLD}	Differential Propagation Delay High to Low	$C_L = 15$ pF $V_{ID} = 200$ mV (Figure 1 and Figure 2)	1.0	1.6	2.5	ns	
t_{PLHD}	Differential Propagation Delay Low to High		1.0	1.7	2.5	ns	
t_{SKD1}	Differential Pulse Skew $t_{PHLD} - t_{PLHD}$ (Note 8)		0	50	400	ps	
t_{SKD2}	Differential Channel-to-Channel Skew-same device (Note 9)		0	0.1	0.5	ns	
t_{SKD3}	Differential Part to Part Skew (Note 10)		0		1.0	ns	
t_{SKD4}	Differential Part to Part Skew (Note 11)		0		1.5	ns	
t_{TLH}	Rise Time				325	800	ps
t_{THL}	Fall Time				225	800	ps
f_{MAX}	Maximum Operating Frequency (Note 13)			200	250		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).

Note 3: All typicals are given for: $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 7 kV

EIAJ (0Ω, 200 pF) ≥ 500V

Note 5: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 6: C_L includes probe and jig capacitance.

Note 7: Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, $Z_O = 50\Omega$, t_r and t_f (0% to 100%) $\leq 3 \text{ ns}$ for R_{IN} .

Note 8: t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.

Note 9: t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.

Note 10: t_{SKD3} , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 11: t_{SKD4} , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as $I_{Max} - I_{Min}$ differential propagation delay.

Note 12: V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN+} and R_{IN-} are allowed to have voltage range -0.05V to $+3.05\text{V}$. V_{ID} is not allowed to be greater than 100 mV when $V_{CM} = 0\text{V}$ or 3V .

Note 13: f_{MAX} generator input conditions: $t_r = t_f < 1 \text{ ns}$ (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), load = 15 pF (stray plus probes).

Parameter Measurement Information

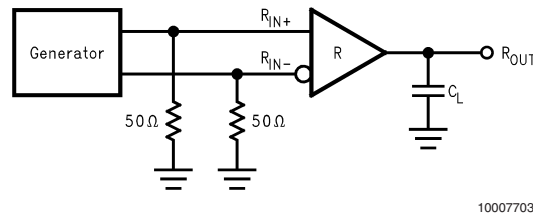


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

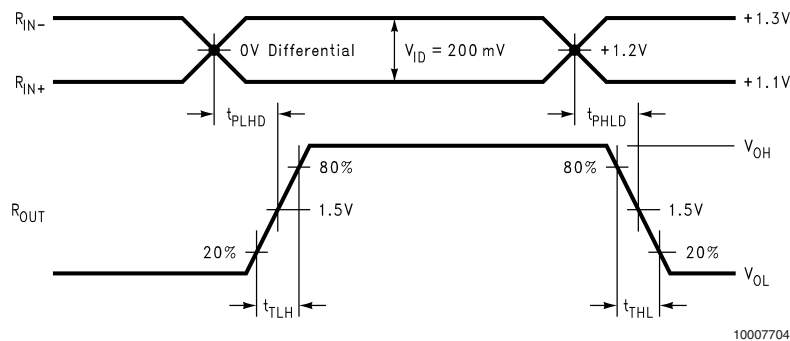


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

Typical Application

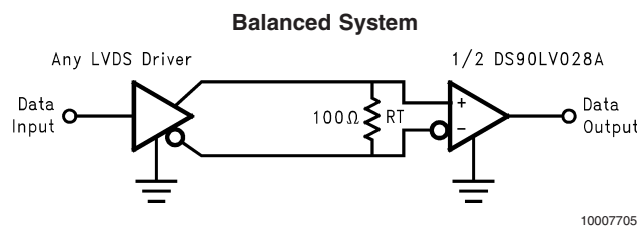


FIGURE 3. Point-to-Point Application

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-002), AN-808, AN-977, AN-971, AN-916, AN-805, AN-903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 3. This configuration provides a clean signaling

environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω . A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other

Applications Information (Continued)

configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV028A differential line receiver is capable of detecting signals as low as 100 mV, over a $\pm 1\text{V}$ common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift $\pm 1\text{V}$ around this center point. The $\pm 1\text{V}$ shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{CC} , but exceeding V_{CC} will turn on the ESD protection circuitry which will clamp the bus voltages.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 μF and 0.01 μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 μF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

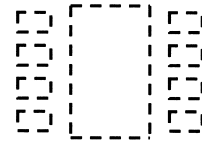
Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

For PC board considerations for the LLP package, please refer to application note AN-1187 "Leadless Leadframe Package." It is important to note that to optimize signal integrity (minimize jitter and noise coupling), the LLP thermal land pad, which is a metal (normally copper) rectangular region located under the package as seen in *Figure 4*, should be attached to ground and match the dimensions of the exposed pad on the PCB (1:1 ratio).

Top View



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FIGURE 4. LLP Thermal Land Pad and Pin Pads

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be $< 10\text{mm}$ long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E$, where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 130 Ω . Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be $< 10\text{mm}$ (12mm MAX).

Applications Information (Continued)

FAIL-SAFE FEATURE

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV028A is a dual receiver device, and if an application requires only 1 receiver, the unused channel inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to

application note AN-1194 "Failsafe Biasing of LVDS Interfaces" for more information.

PROBING LVDS TRANSMISSION LINES

Always use high impedance ($> 100k\Omega$), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances $< 0.5M$, most cables can be made to work effectively. For distances $0.5M \leq d \leq 10M$, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Pin Descriptions

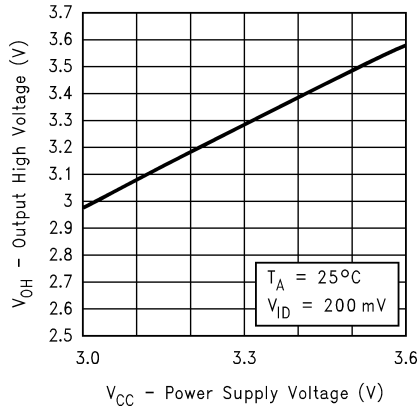
Pin No.	Name	Description
1, 4	R _{IN-}	Inverting receiver input pin
2, 3	R _{IN+}	Non-inverting receiver input pin
6, 7	R _{OUT}	Receiver output pin
8	V _{CC}	Power supply pin, +3.3V ± 0.3V
5	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/Number	Order Number
-40°C to +85°C	SOP/M08A	DS90LV028ATM
-40°C to +85°C	LLP/LDC08A	DS90LV028ATLD

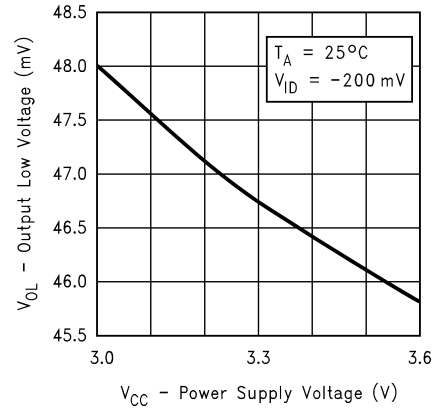
Typical Performance Curves

Output High Voltage vs Power Supply Voltage



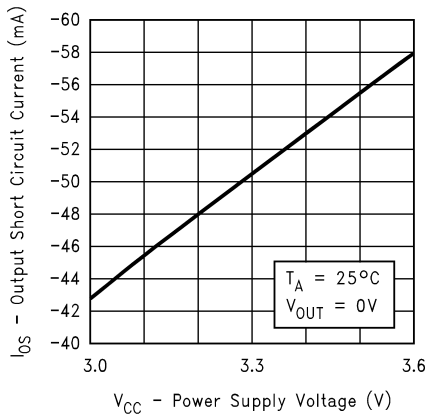
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Output Low Voltage vs Power Supply Voltage



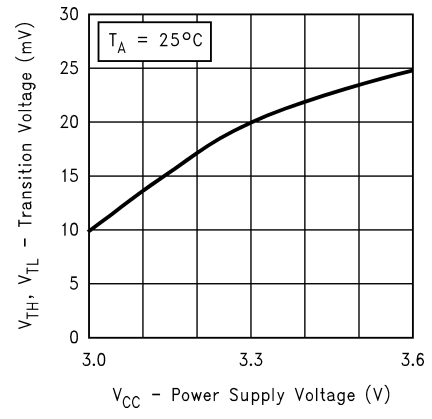
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Output Short Circuit Current vs Power Supply Voltage



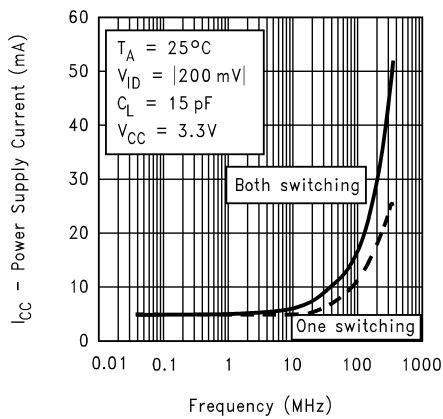
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Differential Transition Voltage vs Power Supply Voltage



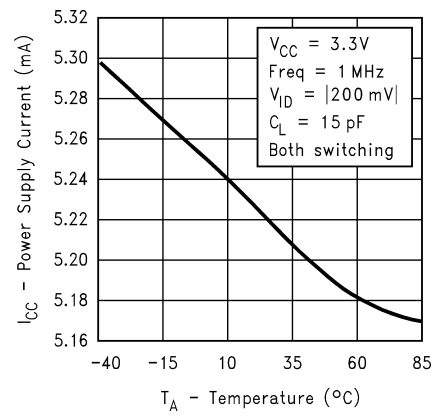
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Power Supply Current vs Frequency



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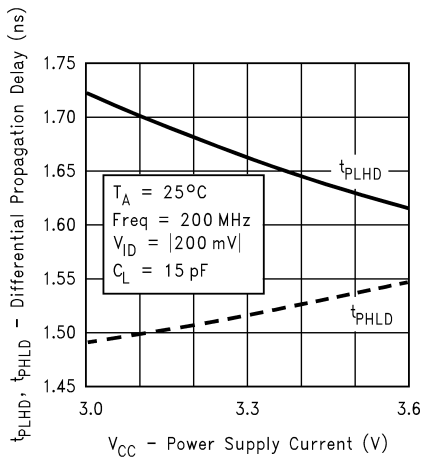
Power Supply Current vs Ambient Temperature



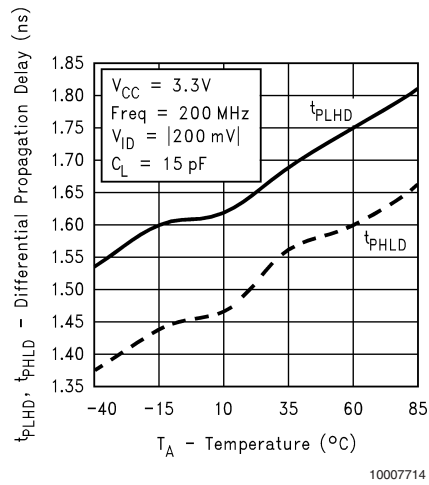
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Typical Performance Curves (Continued)

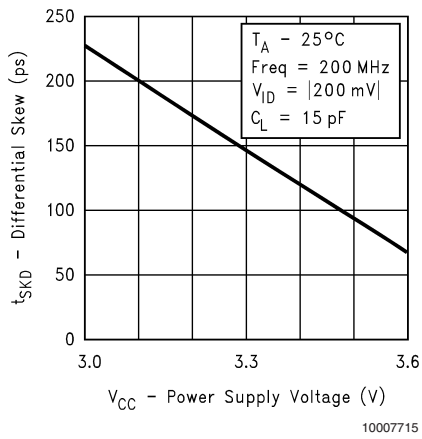
Differential Propagation Delay vs Power Supply Voltage



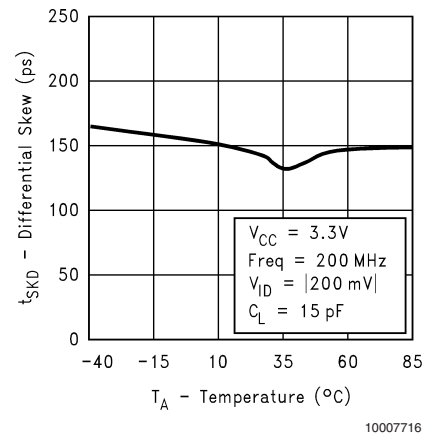
Differential Propagation Delay vs Ambient Temperature



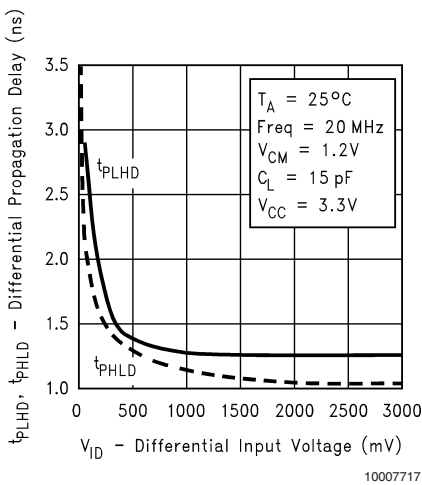
Differential Skew vs Power Supply Voltage



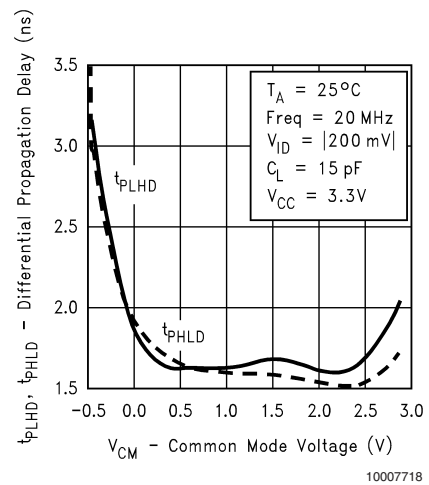
Differential Skew vs Ambient Temperature



Differential Propagation Delay vs Differential Input Voltage

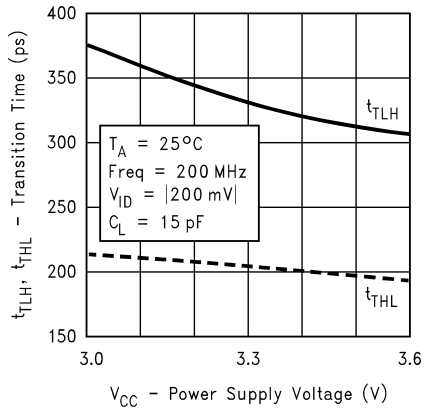


Differential Propagation Delay vs Common-Mode Voltage

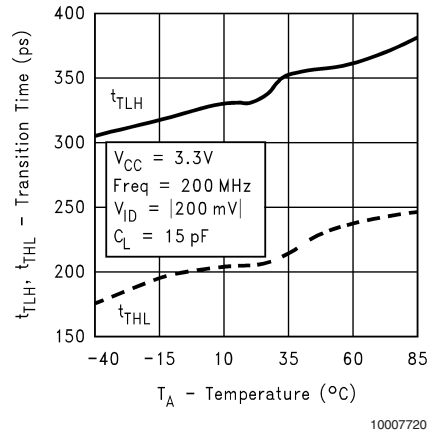


Typical Performance Curves (Continued)

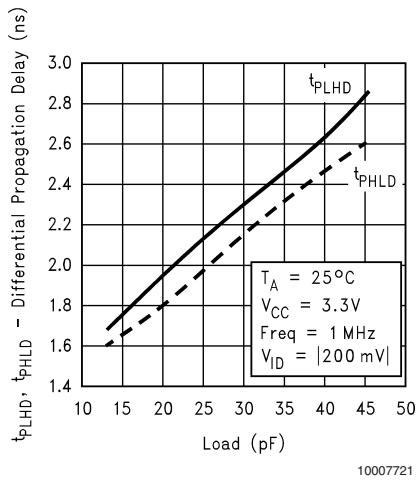
Transition Time vs Power Supply Voltage



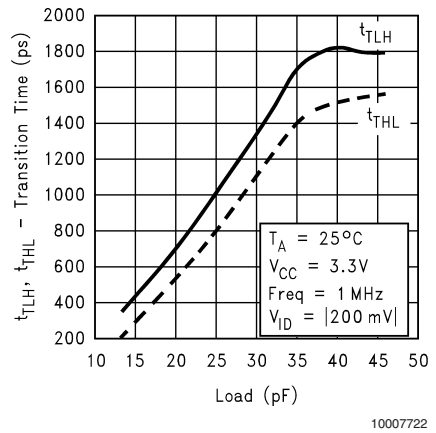
Transition Time vs Ambient Temperature



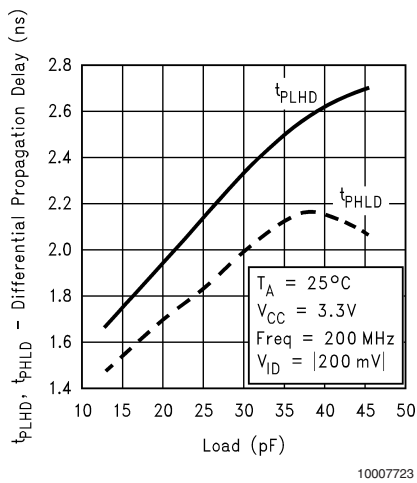
Differential Propagation Delay vs Load



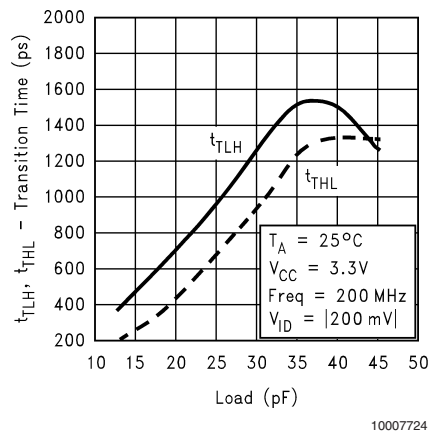
Transition Time vs Load



Differential Propagation Delay vs Load

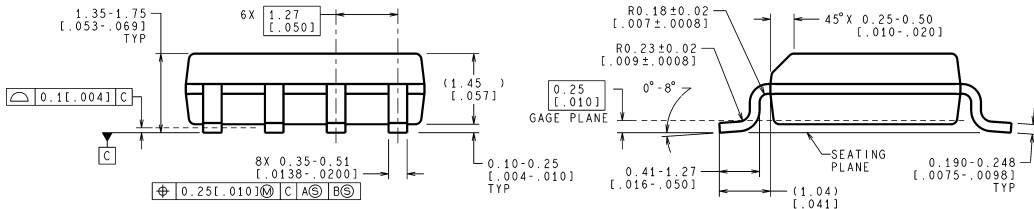
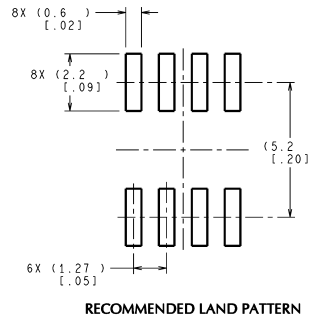
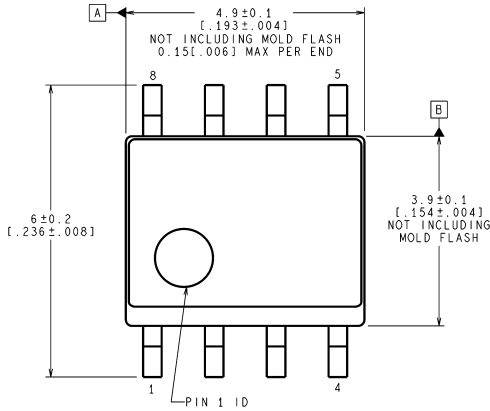


Transition Time vs Load



Physical Dimensions inches (millimeters)

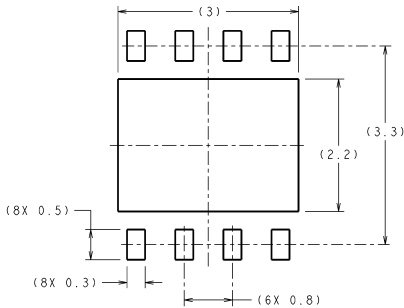
unless otherwise noted



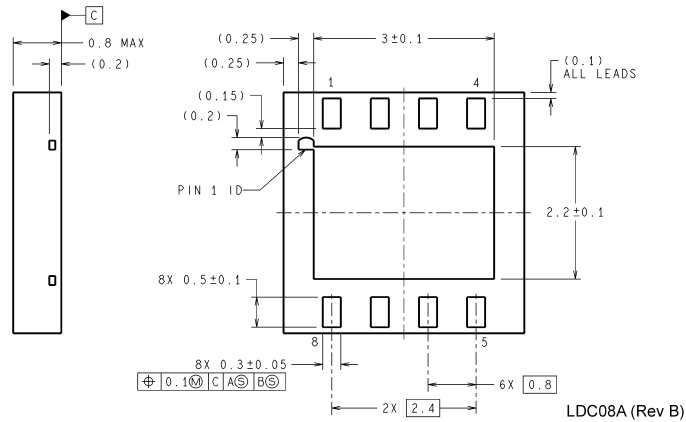
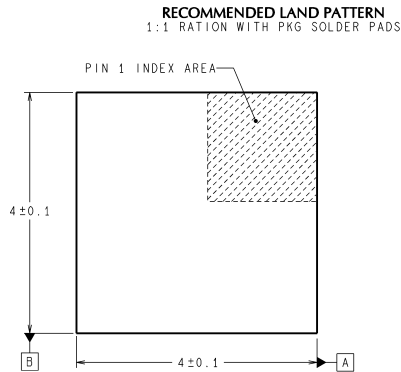
CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [] ARE INCHES
DIMENSIONS IN () FOR REFERENCE ONLY

M08A (Rev K)

8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90LV028ATM
NS Package Number M08A



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



LDC08A (Rev B)

LLP-8, 4mm x 4mm Body
Order Number DS90LV028ATLD
NS Package Number LDC08A

Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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